

AMENDMENT AND RESPONSE

Serial Number: 09/652,998

Filing Date: August 31, 2000

Title: CONTAINER CAPACITOR STRUCTURE AND METHOD OF FORMATION THEREOF

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Docket No. 400.153US07

REMARKS

Claim Rejections Under 35 U.S.C. § 112

Claims 67 and 68 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicant has amended the claims accordingly.

Claim Rejections Under 35 U.S.C. § 103

Claims 13 and 14 were rejected under 35 U.S.C. § 103(a) as being anticipated by Becker et al. (U. S. Patent No. 5,770,498).

Applicant has amended the claims to require that the top capacitor plate does not vertically descend between the first, second and third bottom capacitor plates and the contact.

Claim 13 is substantially different from the cited Becker reference. The capacitor of Becker is substantially similar to the prior art of Figure 2. That is the top electrode descends between the bottom electrodes and the contact. Locating the top electrode in this region encroaches on the lateral spacing of the contact.

Applicants claims reduce this encroachment by prohibiting the top electrode from descending between the bottom electrodes and the contact. Unlike prior art Figure 3, the present claims locate the top electrode in the trench between bottom electrodes. That is, there is capacitive coupling to the interior and exterior of the bottom electrodes, but not in the region between the contact and the bottom electrodes.

Applicant respectfully requests that the claims be allowed.

Claims 67 and 68 were rejected under 35 U.S.C. § 103(a) as unpatentable over applicant admitted prior art in view of Zahurak (U.S. Patent No. 6,150,211).

Claim 67 requires that the top electrode include a lateral clearance opening above the top of the first bottom electrode and around the bit line contact. Further, the top electrode is

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capacitively coupled to an interior of the first, second and third bottom electrodes and a portion of the exterior of the second and third bottom electrodes located in the trench.

Claim 68 also requires that the bit line contact insulation region prevent the top electrode from downwardly extending between the bit line contact and the first and second bottom electrodes.

Figure 2 of the present application illustrates a top electrode descends between the bottom electrodes and the contact (area 5). Locating the top electrode in this region encroaches on the lateral spacing of the contact.

Applicants claims reduce this encroachment by prohibiting the top electrode from descending between the bottom electrodes and the contact. That is, in claim 67 the opening in the top electrode is above the top of the bottom electrode. In claim 68 the top electrode is prohibited from downwardly extending between the bit line contact and the first and second bottom electrodes.

Unlike prior art Figure 3, the present claims locate the top electrode in the trench between bottom electrodes. That is, there is capacitive coupling to the interior and exterior of the bottom electrodes, but not in the region between the contact and the bottom electrodes.

Applicant respectfully requests that the claims be allowed.

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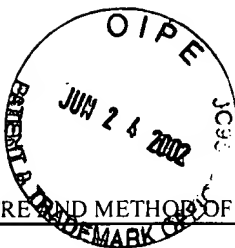
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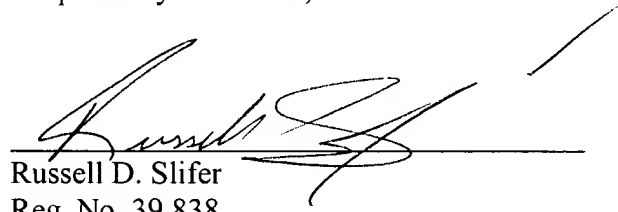


CONCLUSION

Applicant believes that the claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. If the Examiner has any questions regarding this application, please contact attorney Russell D. Slifer at (612) 312-2202.

Respectfully submitted,

Date: 6/24/02


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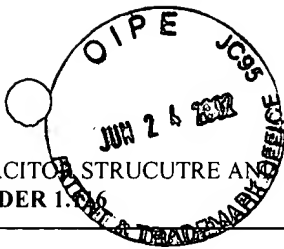
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APPENDIX: Page 1



MARKED-UP VERSIONS OF AMMENDMENTS

IN THE CLAIMS

Please amend the following claims:

13. An array of capacitors, comprising:

a first bottom capacitor plate;

a second bottom capacitor plate;

a third bottom capacitor plate;

a contact between said first bottom capacitor plate and said second bottom capacitor plate, the contact downwardly extends from a vertical height above a top of the first bottom capacitor plate;

a trench between said second bottom capacitor plate and said third bottom capacitor plate;

a common top capacitor plate over said first bottom capacitor plate, said second bottom capacitor plate, and said third bottom capacitor plate, wherein said top capacitor plate extends toward said contact at a first level within said array, the top capacitor plate includes a lateral clearance opening at the first level around the contact and does not vertically descend between the first, second and third bottom capacitor plates and the contact, and wherein said top capacitor plate lines a side of said trench and further lines a bottom of said trench at a second level within said array; and

a dielectric between said top capacitor plate and said first, second, and third bottom capacitor plates.

67. An array of capacitors comprising:

first, second and third memory cell capacitors comprising first, second and third bottom container-shaped electrodes, respectively;

a bit line contact laterally positioned between the first and second memory cell, the bit line contact downwardly extends from a vertical height above a top of the first and second bottom electrodes;

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a trench laterally positioned between the second and third bottom electrodes [to expose a portion of exterior surfaces of the second and third bottom electrodes];

a common top electrode capacitively coupled to the first, second and third bottom electrodes via a capacitor dielectric layer, wherein the top electrode includes a lateral clearance opening above the top of the first bottom electrode and around the bit line contact, the top electrode is capacitively coupled to an interior of the first, second and third bottom electrodes and an portion of the exterior of the second and third bottom electrodes located in the trench; and

a bit line contact insulation region surrounding the bit line contact and filling a region between the bit line contact and the bottom electrode.

68. An array of capacitors comprising:

first, second and third memory cell capacitors comprising first, second and third bottom container-shaped electrodes, respectively;

a bit line contact laterally positioned between the first and second memory cell, the bit line contact downwardly extends from a vertical height above a top of the first and second bottom electrodes;

a trench laterally positioned between the second and third bottom electrodes [to expose a portion of exterior surfaces of the second and third bottom electrodes];

a common top electrode capacitively coupled to the first, second and third electrodes via a capacitor dielectric layer, wherein the top electrode includes a lateral clearance opening around the bit line contact, the top electrode is capacitively coupled to an interior of the first, second and third bottom electrodes and a portion of the exterior of the second and third bottom electrodes located in the trench; and

a bit line contact insulation region surrounding the bit line contact and filling a region between the bit line contact and the first and second bottom electrodes, wherein the bit line contact insulation region prevents the top electrode from downwardly extending between the bit line contact and the first and second bottom electrodes.